

School of Electrical and Computer Engineering

Invites you to the Seminar
Of

Associate Professor Ki Jin Han

Ulsan National Institute of Science and Technology (UNIST), Korea

Friday, November 18th from 1:30 – 3:00 PM in MIRC 102A



“Modeling, Characterization, and Design of Packaging and Interconnections for Advanced Electronic Systems”

Abstract:

With the increase of data bandwidth and the need for multi-functional systems based on higher-level integration, the role of electronic interconnects and packaging (EIP) is becoming more important. The EIP enables the propagation of analog and digital signals in a chip or between sub-systems, but they limit the performance of the entire system especially in high-speed applications due to non-ideal properties such as losses, crosstalk, and impedance mismatching. Therefore, systematic approaches to design EIP, supported by electrical modeling and characterization, are essential for the success in the today's electronic design.

In this talk, the background of the recent EIP research trends will be briefly introduced, and our contributions on the modeling, characterization, and design of EIP will be presented. Firstly, the development of electrical modeling (or path-finding) tool for packages and interposers in silicon-based 3D integration will be discussed. Secondly, indirect contact probing method for the stable and fast characterization of vertical interconnects will be introduced. Finally, design methodologies based on the efficient EIP modeling methods will be presented with high-speed I/O interface design examples.

Biography:

Ki Jin Han received the B.S. and M.S. degrees in electrical engineering from Seoul National University in 1998 and 2000, respectively, and the Ph.D. degree from the Georgia Tech in 2009. From 2009 to 2011, he was with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, as a Postdoctoral Researcher. He is currently with the School of ECE, UNIST, Korea, as an Associate Professor. His current research interests include computational electromagnetics, EMC for power electronics, signal/power integrity for high-speed digital design, antennas, and electrical modeling of electronic packaging and interconnections. Dr. Han served as the TPC Chair of the 2015 IEEE EDAPS Symposium. He received the 2015 IEEE Transactions on Components, Packaging and Manufacturing Technology Best Paper Award in June 2016.

For additional information please contact:

Professor Madhavan Swaminathan (madhavan.swaminathan@ece.gatech.edu) or Pam Halverson (pam@ece.gatech.edu)